

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 14

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte THEODORE W. HOUSTON

Appeal No. 1999-1939
Application No. 08/862,449

ON BRIEF

Before HAIRSTON, JERRY SMITH, and BLANKENSHIP, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 4, 8, 9, 11, 15, 17, 19, 21, 23, 25, 27, 29 and 31.

The disclosed invention relates to an integrated circuit that includes a DRAM device.

Claims 1 and 25 are illustrative of the claimed invention, and they read as follows:

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1. An integrated circuit including a DRAM, said DRAM comprising:

a memory array including a plurality of pass gate transistors and a plurality of memory elements;

said pass gate transistors each having a gate material selected to provide a substantially near mid-gap work function or greater; and

a peripheral area including a plurality of logic transistors.

25. An integrated circuit including a DRAM device, said DRAM comprising:

a memory array including a plurality of pass gate transistors and a plurality of memory elements;

said pass gate transistors comprising n-channel devices having P+ doped polysilicon gate regions; and

a peripheral area including a plurality of logic transistors.

The references relied on by the examiner are:

Klein et al. (Klein) 1972	3,673,471	Jun. 27,
Noguchi 1989	4,841,346	Jun. 20,
Azuma et al. (Azuma) 1989	4,888,631	Dec. 19,
Lee 1992	5,164,805	Nov. 17,
Shino 1993	5,256,894	Oct. 26,
Misawa et al. (Misawa) 1998	5,714,771	Feb. 3,
	(effective filing date May 15,	
1989)		

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We have carefully considered the entire record before us, and we will reverse all of the rejections of record.

All of the claims on appeal require that the pass gate transistors have either "a gate material selected to provide a substantially near mid-gap work function or greater" (claims 1 through 4, 8, 9, 11 and 15) or "n-channel devices having P+ doped polysilicon gate regions" (claims 17, 19, 21, 23, 25, 27, 29 and 31). Inasmuch as the examiner's sole statement (answer, page 3) that "Tanigawa teaches thin film memory cell transistors combined with peripheral transistors" fails to identify which of the transistors in Tanigawa are pass gate transistors, we would have to resort to speculation as to which transistors in Tanigawa are subject to modification based upon the teachings of Lee, Klein, Misawa, Azuma, Shino, Masui or Noguchi. In keeping with In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992), the examiner, and not the Board, bears the initial burden of establishing the prima facie unpatentability of the claimed invention. Thus, we agree with appellant's argument (reply brief, page 2) that the applied references neither teach nor would have suggested the specifically claimed pass gate

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transistors in a DRAM.

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DECISION

The decision of the examiner rejecting claims 1 through
4, 8, 9, 11, 15, 17, 19, 21, 23, 25, 27, 29 and 31 under
35 U.S.C. § 103(a) is reversed.

REVERSED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
)	
)	
)	BOARD OF PATENT
JERRY SMITH)	APPEALS AND
Administrative Patent Judge)	INTERFERENCES
)	
)	
)	
HOWARD B. BLANKENSHIP)	
Administrative Patent Judge)	

KWH:hh

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